Національний технічний університет України
«КИЇВСЬКИЙ ПОЛІТЕХНІЧНИЙ ІНСТИТУТ
імені ІГОРЯ СІКОРСЬКОГО»

Department of Applied Radio Electronics

[RE-121] DESIGN OF DIGITAL DEVICES ON FPGA

Curriculum of the academic discipline (Syllabus)

Course details

Level of higher education	First (bachelor's)
Field of knowledge	17 - Electronics, Automation, and Electronic Communications
Specialization	172 - Electronic Communications and Radio Engineering
Educational program	All educational programs
Discipline status	Elective (F-catalog)
Form of higher education	Full-time
Year of training, semester	Available for selection starting from the 3rd year, fall semester
Scope of the discipline	4 credits (Lectures: 18 hours, Practical classes: 36 hours, Laboratory work: 36 hours, Independent work: 66 hours)
Semester control/control measures	Credit
Class schedule	https://schedule.kpi.ua
Language of instruction	Ukrainian / English
Information about the course coordinator / lecturers	Lecturer: V. S. Mosiychuk, Lab: O. T. Titenko, Independent work: V. S. Mosiychuk
Course location	http://iot.kpi.ua/lms/course/view.php?id=20

Curriculum

1. Description of the course, its purpose, subject matter, and learning outcomes

The purpose of the discipline "Design of Digital Devices on FPGA" is to develop students' abilities to:

- *understand the structure and fundamentals of programmable logic implementation;*
- *understand the syntax and rules of HDL languages for describing digital device models;*
- *understand the differences between structural and behavioral styles of describing digital devices;* • *understand the need and possibilities of testing digital device models using HDL tools;*

- *create combinational digital device models using VerilogHDL;* •
create sequential digital device models using VerilogHDL;
- *create models of complex hierarchical digital device designs and perform their automatic testing.*

After completing the course, students should demonstrate the following learning outcomes:

knowledge:

- the basics of programmable logic implementation;
- syntax and rules for describing digital device models in HDL;
- the capabilities and needs of testing (automatic testing) models of digital devices in HDL;
- concepts for describing complex hierarchical digital systems using HDL hardware description languages.

Skills:

- formulate and understand specifications (technical tasks) for the development of digital devices;
- create projects in an environment for the automatic development of digital device models in HDL; •
implement hierarchical designs of complex digital systems;
- perform optimization of digital device models according to various criteria;

ability to perform certain actions properly, based on the expedient use of acquired knowledge

Experience:

- design and implementation of digital devices on PLDs;
- creation and testing of digital device models using HDL hardware description languages.

2. Prerequisites and post-requisites of the discipline (place in the structural-logical scheme of training under the relevant educational program)

The discipline "Designing CP on FPGA" is based on the following courses: Computer Science, in which students acquired basic programming skills in the C language, Digital Devices, in which students acquired basic concepts regarding basic digital devices.

3. Contents of the course

SECTION 1. Verilog syntax and rules for describing CPU models based on it

Topic 1.1: "Fundamentals of programmable logic, FPGA architecture"

Universal digital devices, examples of programmable CPU implementation on multiplexers and decoders; example of creating a programmable CPU based on ROM; programmable logic arrays (PLAs), programmable matrix logic (PML); example of CPU implementation on PML; modern FPGA structures.

Topic 1.2: "Features of designing digital devices on PLDs. Languages for describing HDL digital device models"

Syntax of the Verilog digital device description language; behavioral description of digital devices; structural description of digital devices; integer, reg, and wire data types; methods for defining logical functions

Topic 1.3: "Description of combinational digital device models in Verilog"

Description of a full adder; description of multiplexers; description of decoders; description of hierarchical digital device designs;

Topic 1.4: "Description of sequential digital device models in Verilog"

The difference between triggers and latches; description of a register; description of a counter with a given counting module; description of a shift register; the difference between blocking and non-blocking assignment;

Topic 1.5: "Features of synchronous CPU implementation"

Definition of synchronous digital devices; recognition of synchronous and asynchronous CPUs; description of

CPUs with synchronous and asynchronous reset; description of Mill and Moore digital automata.

Topic 1.6: "Methodology for testing the functional correctness of CPU models in Verilog"

Methodology for testing and verifying functional correctness; HDL *constructs and directives* that can be used during testing*; outputting information to the console; features of universal test module implementation.*

Topic 1.7: "Description of parametric CPU modules"

Features of describing modules with parameters; for loops and others that can be synthesized in parametric modules; parameterization of the pseudorandom code generator module; example of complete parameterization of the PRS generator module;

Topic 1.8: "Features of creating a pipeline-type CPU"

Time and space parallelism – analogies from real life; assessment of performance improvement through parallelism; description of a digital filter, analysis of the complexity of its individual blocks; optimization of a digital filter, implementation of a conveyor-based adder;

Topic 1.9: "Features of designing CPUs resistant to needle-type interference"

Time characteristics of digital devices; nature of needle-type interference; description and use of external signal input synchronizers; correct circuits for edge detection and pulse formation using a gated clock signal.

SECTION 2. *Description and testing of digital device models in Verilog*

Topic 2.1. Implementation of a combinational CPU on a FPGA.

Description of a combinational CPU in behavioral and structural style. Testing of the module using a created automatic testing module. Assignment of FPGA output ports and configuration of the FPGA on the board.

Topic 2.2. Implementation of a sequential CPU on an FPGA.

Description of sequential CP in behavioral and structural style. Testing of the module using the created automatic testing module. Assignment of FPGA output ports and configuration of FPGA on the layout.

Topic 2.3. Implementation of a parallel interface to the DAC. Formation of specified signals

Creation of a hierarchical project in a structural style. Creation of a test plan and its implementation in an automatic testing module. Assignment of FPGA output ports and configuration of the FPGA on the layout.

Topic 2.4. Implementation of a digital filter on an FPGA.

Creating a hierarchical project with a digital filter. Optimizing the combinational filter circuit based on the creation of a pipeline. Assigning ports to FPGA outputs and configuring the FPGA on the board.

4. Training materials and resources

Basic

1. Description and simulation of digital device models in Verilog: Method. Instructions for performing computational and graphical work for students majoring in "Radio-electronic devices and equipment."
"Intelligent Technologies of Microsystem Radioelectronic Engineering," "Biotechnical and Medical Devices and Systems" / Compiled by: V.S. Mosiychuk. – Kyiv: NTUU "KPI," 2012. – 35 p. – Access mode: http://ros.kpi.ua/downloads/CXT_EA_RGR.pdf

2. Ryabenkyi V. M. VERILOG. Practice of designing digital devices on FPGA: Tutorial. / V. M. Ryabenkyi, O. O. Ushkarenko; Admiral Makarov National University of Shipbuilding. - Mykolaiv: Ilion, 2007. - 324 p.

Supplementary

3. Harris D. M. Digital Design and Computer Architecture / D.M. Harris, S. L. Harris. ; Sec. Ed. - Morgan Kaufmann, 2013. - 560 p. - ISBN 978-0-12-394424-5.]. - Access mode:

https://www.uop.edu.jo/download/research/members/Digital_Design_and_Computer_Architecture.pdf
4. Ciletti M. D. Advanced Digital Design with the Verilog HDL / M.D. Ciletti. – Prentice Hall. – 982 p. – ISBN 978-0-13-089161-7.

Information resources

5. Altera Corporation [Electronic resource]. – Access mode: http://altera.com. – Title from the screen.

6. Designing digital devices: a selection of e-books [Electronic resource]. – Access mode: http://www.ex.ua/12183571. – Title from the screen.

Educational content

5. Methodology for mastering the academic discipline (educational component)

4. Lectures

No	Lecture topic and list of main questions (list of teaching aids, references to literature, and assignments for independent study)
1	*Topic: "Fundamentals of programmable logic, FPGA architecture"* *universal digital devices, examples of programmable CPUs implemented on multiplexers and decoders;* • *example of creating a programmable CPU based on a PDP;* • *programmable logic arrays (PLAs), programmable matrix logic (PML);* • *example of CPU implementation on PML;* *modern FPGA structures.* *Literature:* • *Horowitz P., Hill W. The Art of Circuit Design, Chapters 8.15, 8.27* *Maxfield, K. Designing with FPGAs: A Beginner's Guide, Chapters 2, 3, 4* *Assignment for independent study:* • *Research the history of the creation of languages for describing digital device models.* *Familiarize yourself with the international standards for the two most common languages for describing digital devices, VHDL and VerilogHDL*
2	*Topic: "Features of designing digital devices on FPGA. Languages for describing HDL digital device models"* • *Syntax of the Verilog language for describing digital devices;* • *behavioral description of digital devices;* • *Structural description of digital devices;* • *integer, reg, and wire data types;* *methods for defining logical functions.* *References:* • *Polyakov A. K. VHDL and VERILOG languages in digital equipment design, Chapters 1, 2.* • *Harris D. M.* Digital Design and Computer Architecture, ch. 4 • *Ciletti M. D.* Advanced Digital Design with the Verilog HDL, ch. 4 *Assignments for independent study:* • *Write down the basic logical elements of Verilog with examples in your notes.*
3	*Topic: "Description of combinational digital device models in Verilog"* • *description of a full adder;* • *description of multiplexers;* • *description of decoders;* *description of hierarchical designs of digital devices;* *References:* *Polyakov A. K. VHDL and VERILOG languages in digital equipment design, Sections 3.1, 5.6.* • *Harris D. M.* Digital Design and Computer Architecture, ch. 2, 4.2, 4.3. 4.5 • *Ciletti M. D.* Advanced Digital Design with the Verilog HDL, pp. 143-149; ch. 6.2 *Assignments for independent study:* *Describe in structural style an 8-bit comparator based on a single-digit comparator;*

4	*Topic: "Description of serial digital device models in Verilog"* • *difference between the description of triggers and latches (locks);* • *description of a register;* • *description of a counter with a given counting module;* • *Description of a shift register* *The difference between blocking and non-blocking assignment. References:* *Polyakov A. K. VHDL and VERILOG languages in digital equipment design, Sections 3.2, 5.7.* • *Harris D. M.* Digital Design and Computer Architecture, ch. 3, 4.4 • *Ciletti M. D.* Advanced Digital Design with the Verilog HDL, pp. 150-223, ch. 6.3 *Assignment for independent study:* • *Describe a reversible counter with an arbitrary counting module in HDL.*

5	*Topic: "Features of synchronous CPU implementation"* • *Definition of synchronous digital devices;* • *Recognition of synchronous and asynchronous CPUs;* • *description of CPUs with synchronous and asynchronous reset;* *description of Mil and Moore digital automata.* *References:* • *Polyakov A. K. VHDL and VERILOG languages in digital equipment design, Ch. 3.3, 5.8* • *Harris D. M.* Digital Design and Computer Architecture, ch. 3.3-3.4, 4.6 • *Ciletti M. D.* Advanced Digital Design with the Verilog HDL, ch. 6.5-6.7 *Assignments for independent study:* *Describe a digital machine that will implement the state diagram of a washing machine machine.*
6	*Topic: "Methodology for testing the functional correctness of CPU models in Verilog"* • *methodology for testing and verifying functional correctness;* • HDL *constructs and directives* that can be used during testing*;* • *outputting information to the console;* • *Features of implementing universal test modules. References:* • *Polyakov A. K. VHDL and VERILOG languages in digital equipment design, Chapter 4* • *Maxfield K. Designing with FPGAs: A Beginner's Guide, Chapter 19* • *Harris D. M.* Digital Design and Computer Architecture, ch. 4.8 *Assignments for independent study:* • *Describe a test module for automatic verification of the functional correctness of a comparator and a reversible counter.* *correctness of the comparator and the reversible counter.*
7	*Topic: "Description of CPU parametric modules"* • *Features of describing modules with parameters;* • *for digits, etc., which can be synthesized in parametric modules;* • *parameterization of the pseudorandom code generator module;* *example of complete parameterization of the PRNG module;* *References:* • *Maxfield K. Designing with FPGAs. A Beginner's Guide, pp. 361-376* • *Harris D. M.* Digital Design and Computer Architecture, ch. 4.7 • *Ciletti M. D.* Advanced Digital Design with the Verilog HDL, ch. 5.10 *Assignment for SRC:* • *Describe the parameterized CPU modules in accordance with the design task.*
8	*Topic: "Features of creating a pipeline CPU"* • *Temporal and spatial parallelism – analogies from real life;* • *assessment of performance improvement through parallelism;* • *description of a digital filter, analysis of the complexity of its individual blocks;* • *optimization of a digital filter, implementation of a conveyor-based adder; Literature:* • *Maxfield K. Designing with FPGAs. A Beginner's Guide, Chapters 7, 12* • *Harris D. M.* Digital Design and Computer Architecture, ch. 3.6 • *Ciletti M. D.* Advanced Digital Design with the Verilog HDL, ch. 9.3-9.5 *Assignment for independent study:* *Consider possible options for implementing a pipeline-type digital filter, assess the degree of performance optimization.*
9	*Topic: "Features of CPU design resistant to needle-type interference"* • *Time characteristics of digital devices;* • *nature of needle-type interference;* • *description and use of external input signal synchronizers;* *correct circuits for edge detection and pulse formation using a gated clock signal.* *References:* • *Harris D. M.* Digital Design and Computer Architecture, ch. 3.5 • *Ciletti M. D.* Advanced Digital Design with the Verilog HDL, ch. 2.5, 6.11 *Assignment for independent work:* • *Consider the practical use of synchronizers in the project in accordance with the design specification*

Laboratory classes

Since the discipline "CPU Design on FPGA" belongs to **the cycle of disciplines** of **professional and practical** training, considerable attention is paid to the practical component of training. The main purpose of the laboratory classes is to experimentally verify theoretical knowledge, acquire design skills, implement algorithms based on Verilog HDL description languages, test and verify radio engineering device designs by modeling them and configuring FPGAs on mockups.

No.	Name of laboratory work	Number Class hours
1	*Description and testing of a combinational CPU. Programming on FPGA*	4
2	*Description and testing of sequential CPUs. Programming on FPGA.*	4
3	*Description and testing of a digital interface to a DAC. Creation signal generator with a specified waveform*	4
4	*Description and testing of the digital interface to the ADC. Implementation of a digital filter. Discretization of an analog signal, its digital filtering and reproduction on a DAC*	4

All laboratory work is performed in the Quartus II automated design environment on training models with Altera FPGA. Each student receives an individual assignment, which they complete independently at their workstation, equipped with a personal computer and an FPGA model. Students receive their laboratory assignments in advance. Before the start of the class, a survey is conducted to assess the student's readiness to perform the work. After completing the work, the results are defended and discussed.

Laboratory work is planned after studying the main material, as laboratory work is complex.

6. Independent work of the student

No.	Title of the topic for independent study	Number hours SRC
1	*Topic 6: "Methodology for testing the functional correctness of CPU models in Verilog"* • *drawing up a test plan;* *creating modules for automatic verification of the functional correctness of the hierarchical CPU module;* *References:* • *Harris D. M.* Digital Design and Computer Architecture, ch. 4.8	6
2	*Topic 7: "Description of CPU parametric modules"* *parameterization of individual modules of a hierarchical design in accordance with the design task;* *Modification of combinational circuits with the possibility of building a pipeline in accordance with the design task* References: *Ciletti M. D.* Advanced Digital Design with the Verilog HDL, ch. 5.10 • *Harris D. M.* Digital Design and Computer Architecture, ch. 4.7	6

Homework

The main objectives of the homework assignment are to develop skills in independently managing your own project, in particular, the development of a radio engineering device using PLDs.

Each individual DCR task is a specification for a digital device. The specification describes the functionality to be implemented. It may also include the structure of the project and the implementation path for a particular digital device.

In accordance with the DTR task, the project should consist of two parts: modules describing the functional model of the digital device and an automatic testing module that verifies the project. To verify the project, you need to develop a test plan, describe the test module (testbench), and determine the expected simulation results. At a minimum, the test plan should describe: 1) the functional features to be tested; 2) how these features should be tested.

Typical tasks for Home Control Work

1. Develop and verify on Verilog state diagrams and behavioral models of the Miller and Moore automata, ensuring detection of the value 01002 in the stream, starting from the least significant bit.
2. Develop and test a model of a 4-bit counter, which, depending on the control signal model, will be able to count in binary code or Gray code.
3. Develop a finite state machine with clk and reset inputs and clk_by_6 and clk_by_10 outputs (clock frequency divider by 6 and 10, respectively).
4. Develop a behavioral model of the frequency divider module by 11 "Divide_by_11".
5. Describe the model of the module for determining data that is not in binary-decimal encoding format.
6. Develop, test, and synthesize a Moore digital automaton for recognizing the code sequence "001011" in a stream.
7. Develop, test, and synthesize a digital Milly machine for recognizing the code sequence "001011" in a stream.
8. Using continuous assignment, develop and test a comparator model that can compare four 32-bit unsigned binary numbers and generate an output signal that indicates which of the numbers is the largest and which is the smallest.
9. Using the always block, develop and test a behavioral model of a comparator that can compare four 32-bit unsigned binary numbers and generate an output signal that indicates which of the numbers is the largest and which is the smallest.
10. Describe the model and confirm the functionality of a cyclic shift register. Such registers are used in signal processors to avoid overflow problems due to arithmetic operations and allow values to be scaled. Thus, in the case of a 1-bit shift to the left, the value is multiplied by 2, and in the case of a shift to the right, it is divided. The shift operation can be implemented with a combinational circuit, but the task requires the use of an additional register.
11. Describe in Verilog and verify the circuit shown below. The output P_odd will be 1 at the output if the values at the input D_in, which follow one another, are not the same.
12. Develop and verify a 4-bit Johnson counter model in Verilog.

Policy and control

7. Academic discipline policy (educational component)

Rules for attending classes (both lectures and practical/laboratory classes)

Laboratory work is mandatory. If these classes are missed, they must be made up during consultations or with other groups. If lectures are missed, tests on the material covered in the missed class must be taken and passed. Lecture materials and videos are posted on the LMS.

Defense of laboratory work

Laboratory work is defended on the day the laboratory work is completed. The student receives two grades. The first is for activity and initiative during the laboratory work and individual classes. The second is for the defense and answers to control questions.

Defense of individual assignments

As part of their independent work, students complete assignments based on lecture materials. Based on the results of the review, course participants receive comments from the instructor and a grade. Individual assignments cannot be retaken.

Incentive and penalty points and academic integrity policy

The most active students and students who complete individual assignments in an exemplary manner can receive up to 10 points towards their semester grade.

Penalty points are applied in cases where someone else's work is presented as their own, with mandatory subsequent reworking.

Deadline and resit policy

If the deadlines for submitting assignments are missed, the maximum score for the assignments is reduced by 10%.

8. Types of control and rating system for assessing learning outcomes.

Rating system

- Lectures/webinars - 18 hours; (*3 Home Control Work x 10 points*)
- Practical work/training - 18 hours; (*6 assignments x 5 points*) • Laboratory work - 18 hours; (*4 labs x 5 points*)
- Homework assignment (*1 project x 20 points*)

Table of correspondence between rating points and university scale grades

Number of points	Grade
100-95	Excellent
94-85	Very good
84-75	Good
74-65	Satisfactory
64-60	Sufficient
Less than 60	Unsatisfactory
Admission requirements not met	Not admitted

9. Additional information on the discipline (educational component) List of questions and tasks for the test

1. Describe a 4-bit shift register in VerilogHDL.
2. Verilog "assign" and "always" constructs.
3. Spatial and temporal parallelism. Conveyor structure of digital devices.
4. Styles of describing combinational circuits in VerilogHDL.
5. Describe a combinational circuit in VerilogHDL using behavioral style, using a single- bit half-adder as an example.
6. Time characteristics of combinational circuits: t_{cd} and t_{pd}
7. Time characteristics of sequential digital devices (t_{setup}; t_{hold}; t_{ccd}; t_{pcd}).
8. Synchronous digital devices. Basic rules of synthesis. Clock signal and phase shift (clock skew).
9. Finite (digital) automata. Methods of describing finite automata. Moore and Miller automata.
10. Verilog designs for describing CPUs and for simulation.
11. Describe an 8-function ALP in VerilogHDL.
12. Synchronization in digital devices. Clock pulse multiplication.
13. Needle-type interference in combinational circuits, causes and methods of combating it.
14. Conditions under which a circuit can be considered combinational.
15. What is the difference between latches and flip-flops?
16. Synchronization in digital devices. Synchronization pulse parameters (t_{setup} ; t_{hold} ; t_{ccd} ; t_{pcd}).

17. Describe a Moore finite state machine for detecting the code sequence 1010 in VerilogHDL.
18. Synchronous and asynchronous circuits, classification.
19. Front and rear pulse edge detectors.
20. Describe an asynchronous counter M= 6.. on VerilogHDL.
21. Synthesis of pulse distributors.
22. Schematic diagrams of a D flip-flop.
23. Describe a 5-bit synchronous accumulator counter in VerilogHDL.
24. Single-digit full adder. Description in VerilogHDL.
25. Describe a binary code converter to a seven-segment indicator code in VerilogHDL.
26. Describe memory registers with parallel and serial data recording in VerilogHDL.
27. Describe a JK flip-flop model in Verilog.
28. Describe a synchronous accumulator counter with a count module of 10 in VerilogHDL.
29. Describe a reversible synchronous counter in VerilogHDL.
30. Describe a binary code decoder into a seven-segment display in VerilogHDL.
31. Structural description of combinational circuits in VerilogHDL
32. ALP. Structural diagram of ALP for 8 functions.
33. Time characteristics of sequential digital devices (t_{setup} ; t_{hold} ; t_{ccd} ; t_{pcd}).
34. General block diagram of a finite state machine.
35. Describe the multiplexer model in behavioral and structural styles.
36. Describe basic logic elements in VerilogHDL.
37. Describe a sequential multi-digit adder in VerilogHDL.
38. Describe a synchronous counter with a count module of 9 in VerilogHDL.
39. Describe a subtracting synchronous counter with a count module of 10 in VerilogHDL.
40. Parallel adder with parallel carry.
41. Describe a D-type flip-flop model with leading and trailing edge switching.
42. Describe the model of an accumulating adder.
43. Describe a model of an accumulating counter with preliminary asynchronous setting in VerilogHDL.
44. Describe an 8-to-3 decoder in VerilogHDL.
45. Describe a circuit for comparing bits A > B in Verilog.
46. Describe a multiplexer with 4 address inputs in VerilogHDL.
47. Describe a binary code to Gray code converter in VerilogHDL.
48. Describe a Moore finite state machine for detecting the code sequence 110101 in VerilogHDL.
49. Describe a Mealy finite state machine for detecting the code sequence 1011 in VerilogHDL.
50. Describe a multiplexer with 8 data inputs in VerilogHDL.
51. Describe an asynchronous subtracting counter M = 5 in VerilogHDL.
52. Describe a combinational circuit based on a logical function in Verilog.
53. Describe a synchronous counter with M = 5 in Verilog.
54. Describe a combinational circuit in behavioral style using Verilog.
55. Describe a circuit for comparing bits A ≥ B in Verilog.
56. Describe an 8-bit register with parallel data entry in VerilogHDL.
57. Describe a circuit for comparing two 2-bit numbers A ≤ B in Verilog.
58. Describe a 2-to-4 encoder in VerilogHDL.
59. Describe a circuit for comparing bits A < B in Verilog.
60. Describe a counter with M = 7 in VerilogHDL.
61. Synthesize a summing counter with states 3,4,5,6,7,3.1
62. Describe a Milly automaton circuit in VerilogHDL using a state diagram.
63. Describe a summing counter with M = 5 in Verilog.
64. Describe a 3-bit binary code to Gray code converter in VerilogHDL.
65. Describe a D-flip-flop in VerilogHDL
66. Describe a summing counter with M = 7 in VerilogHDL.
67. Describe a comparator for two two-digit numbers A ≠ B in Verilog.
68. Describe a comparator with output A = B in VerilogHDL.
69. Describe a 4-bit adder in VerilogHDL using the previously described full adder module.

Description of material, technical, and information support for the discipline

Laboratory work is carried out in a specialized laboratory 510b-17. It is equipped with 8 workstations with models based on ALTERA ACEX10 FPGA.

Work program for the academic discipline (syllabus):

Compiled by V. S. Mosiychuk; O. T. Titenko;

Approved by the PRE Department (Minutes No. 06/2024 dated 06/27/2024)

Approved by the methodological commission of the faculty/research institute (protocol No. 06/2024 dated 28.06.2024)