National Technical University of Ukraine
“Igor Sikorsky Kyiv Polytechnic Institute”

Department of Radio Engineering Systems

INFORMATICS. PART 2.
FUNDAMENTALS OF COMPUTER TECHNOLOGY

SYLLABUS

for technical specialties at Igor Sikorsky KPI

DETAILS OF THE ACADEMIC DISCIPLINE

Level of higher education First (bachelor's)

Field of knowledge	G - Engineering, manufacturing, and construction
Special	G5 "Electronics, electronic communications, instrument engineering, and radio engineering"
Educational program	1.Intelligent technologies of radio electronics 2.Information and Communication Radio Engineering 3.Radio Engineering Computerized Systems 4.Radio Electronic Warfare Technologies
Status of discipline	Specialized
Form of study	Full-time (day)
Year of training, semester	1st year, 2nd semester
Scope of the discipline	4/120 (30 hours – lectures, 30 hours – laboratory lessons, 60 hours – independent work)
Semester control/control measures	Test/Module test /homework test
lesson schedule	http://rozklad.kpi.ua
Language of instruction	Ukrainian
Information **Course director / lecturers**	Lecturer: Ihor Tovkach, PhD, Senior Lecturer Lab.works: Sergey Borisovich Mogilny, PhD, Associate Professor,isearch@ukr.net , +38(068)071-22-25.
Course location	https://iot.kpi.ua/lms

ACADEMIC DISCIPLINE PROGRAM

1. Description of the academic discipline, its purpose, subject matter, and learning outcomes

1.1. Description of the academic discipline

The academic discipline consists of one section

1.2. Purpose of academic discipline

The purpose of the academic discipline is to train specialists who have basic competencies in developing implementation schemes for combinational and sequential digital devices based on logical functions.

The purpose of the academic discipline is to develop **the following competencies** in students:

- Ability to apply knowledge in practical situations (GC 02).
- Knowledge and understanding of the subject area and understanding of professional activity (GC 04).
- Ability to learn and acquire modern knowledge (GC 07).
- Ability to identify, pose, and solve problems (GC 08).
- Ability to solve standard tasks of professional activity based on information and bibliographic culture with the use of information and communication technologies and taking into account the principles of using information and communication technologies and taking into account the basic requirements of information security (PC 02). basic information security requirements (PC 02).

Ability to perform computer modeling of devices, systems, and processes using universal application software packages (PC 04).

1.3. Subject of study

The subject of the discipline *is* a set of solutions in mathematical logic and the description in HDL of the basic elements of the CPU, methods for minimizing logical functions for the implementation of combinational CPUs in different bases, methods for analyzing the operation of the CPU to verify the implementation of specified logical functions and time parameters.

1.4. Program learning outcomes

- Find, evaluate, and use information from various sources necessary for solving professional tasks, including reproducing information through electronic search. (PRO 18).

2. Prerequisites and post-requisites of the discipline

The educational component "Computer Science" is taught in the first semester of the first year of study for students enrolled in the educational program "Intelligent Technologies in Radio Electronics." The competencies acquired by students in the course of studying this discipline are applied in the mastery of the discipline "Programmable Tools in Intelligent Radio Electronics."
Prerequisites for studying this discipline are "General Physics" and "Analytical Geometry and Linear Algebra."

3. Contents of the discipline

Topic 1. Mathematical foundations of digital signal processing devices.

Topic 2. Automation of logical function minimization.
Topic 3. Synthesis of logic circuits on multiplexers.
Topic 4. Serial digital devices.
Topic 5. Registers and binary counters.
Topic 6. Synthesis of synchronous and asynchronous sequential devices.
Topic 7. Mill and Moore digital automata.
Topic 8. Arithmetic devices.
Topic 9. Digital-to-analog and analog-to-digital converters.

4. Teaching materials and resources

Basic literature:

1. Mogilny S.B. Informatics. Part 2. Fundamentals of Computer Science: Laboratory Practicum [Electronic resource]: textbook for bachelor's degree students majoring in 172 "Electronic Communications and Radio Engineering" / S.B. Mogilny, L.D. Orkush; Igor Sikorsky Kyiv Polytechnic Institute. – Electronic text data (1 file: 2.3 MB). – Kyiv: Igor Sikorsky Kyiv Polytechnic Institute, 2023. – 84 p. – Title from the screen.

1. Ryabenkyi V. M., Zhuykov V. Ya., Gulii V. D. Digital Circuitry: Textbook. - Lviv: "Novyi Svit-2000," 2020. – 736 p.

2. Matvienko M. P. Designing Digital Devices. - Kyiv: Lira-K, 2018, - 364 p.

3. Analysis, synthesis, and design of digital control systems: textbook / S. M. Yesaulev, O. F. Babicheva; Kharkiv National University of Municipal Economy named after O. M. Beketov. – Kharkiv: O. M. Beketov National University of Urban Economy, 2018. – 150 p.

4. Vorobyova O.M. Digital devices: textbook. – Part 2 / O.M. Vorobyova, M.P. Savitska, Yu.V. Fleita. – Odessa: O.S. Popov Odessa National Academy of Civil Engineering and Architecture, 2016. – 80 p.

5. Medvedyk, A.D. Circuitry of Digital Devices: Textbook. Collection of Problems. Odessa National Polytechnic University – Odessa: Nauka i Tekhnika, 2009. – 322 p.

Additional literature:

1. Radio Engineering: Encyclopedic Educational Reference Book: Textbook / Edited by Yu. L. Mazor – Kyiv: Vyshcha Shkola, 1999. –839 p.

2. James M. Lee. Verilog Quickstart. A Practical Guide to Simulation and Synthesis in Verilog/ Third edition: - Cluwer Academic Publishers. 2002. – 355 p.

Internet information resources:

1. Distance learning website on the Moodle platform of the Mikrotik Academy: - http://iot.kpi.ua/lms/
2. Sikorsky distance learning platform: - https://www.sikorsky-distance.org/

EDUCATIONAL CONTENT

5. Methodology for mastering academic discipline (educational component)

5.1. Distribution of lessons by topic

Topic 1. *Lecture 1*. Basic laws of algebraic logic
Lecture 2. The concept of combinational digital circuits.
Topic 2. *Lecture 3.* Automation of logical function minimization.
Lecture 4. Description and implementation of simple combinational device circuits.
Topic 3. *Lecture 5.* Combinational devices with Verilog descriptions.
Lecture 6. Synthesis of combinational device circuits.
Topic 4. *Lecture 7*. Triggers.
Lecture 8. Triggers with signal edge clocking.
Topic 5. *Lecture 9.* Registers, binary counters.
Topic 6. *Lecture 10.* Synthesis of synchronous sequential devices.
Lecture 11. Synthesis of asynchronous sequential devices.
Topic 7. *Lecture 12*. Mil and Moore synchronous digital automata, description in Verilog.
Lecture 13. Arithmetic devices.
Lecture 14. Performing multiplication operations.
Topic 9. *Lecture 15*. Digital-to-analog and analog-to-digital converters.

Modular control work (MCW) (tests for distance learning):
1. On topic 7.
Preparation for the test

5.2. Methodology of mastering

Lectures

Lecture 1. Basic laws of algebraic logic

Lecture content:

1. The concept of a logical function and the laws of Boolean algebra.
2. Logical operators in the Verilog language.
3. Potential coding, the concept of a defining potential.

Lecture 2. The concept of combinational digital circuits

Lecture content:

1. Elementary combination circuits: half-adder, single-bit adder, decoder.
2. Implementation of combinational devices in different bases.

Lecture 3. Automation of logical function minimization

Lecture content:

1. Using Karnaugh maps to minimize logical functions.
2. Features of minimization when there are more than four arguments.

Lecture 4. Description and implementation of simple combinational device circuits

1. Description of a half-adder and adder in Verilog.
2. Encryptor, decryptor, electronic switches.

Lecture 5. Combinational devices with description in Verilog

Lecture content:

1. Multiplexers.
2. Code converters.
3. Description of multiplexers and code converters in Verilog.

Lecture 6. Synthesis of combinational device circuits

Lecture content:

1. Synthesis of multiplexer circuits using Karnaugh maps.
2. *Case* and *if* structures for describing combinational devices in Verilog.

Lecture 7. Triggers

Lecture content:

1. Sequential devices.
2. RS flip-flops.
3. D-flip-flop, T-flip-flop.

Lecture 8. Triggers with signal difference clocking

Lecture content:

1. Triggers with internal delay: RS triggers, JK trigger.
2. Description of triggers in Verilog.
3. Dynamic flip-flop.

Lecture 9. Registers, binary counters

Lecture content:

1. Registers: serial, parallel, universal.
2. Description of registers in Verilog.
3. Synchronous and asynchronous binary counters.
4. Description of binary counters in Verilog.

Lecture 10. Synthesis of synchronous sequential devices

Lecture content:

1. Methods for synthesizing synchronous counters with arbitrary count modules.
2. Description of synchronous counters with arbitrary counting modules in Verilog.

Lecture 11. Synthesis of asynchronous sequential devices

Lecture content:

1. Synthesis of asynchronous counters with arbitrary counting modules.

Lecture 12. Synchronous digital automata of Mil and Moore, description in Verilog

Lecture content:

1. Construction of a directed graph of a digital automaton (DA).
2. Construction of a DA on triggers with minimization of logical functions.
3. Description of CA in Verilog using a directed graph.

Lecture 13. Arithmetic devices

Lecture content:

1. Multi-digit adders.
2. Arithmetic logic unit.

Lecture 14. Performing multiplication operations

Lecture content:

1. Basic methods of performing multiplication of numbers.
2. Methods for accelerating multiplication of numbers.

Lecture 15. Digital-to-analog and analog-to-digital converters

Lecture content:

1. Methods of digital-to-analog (DAC) and analog-to-digital (ADC) signal conversion.
2. DAC and ADC circuits: successive approximation, double integration, parallel.

3. The principle of sigma-delta ADC construction

Laboratory work

Laboratory work 1. Investigation of a laboratory model for hardware simulation of logic circuits

Theoretical part

Familiarization with the capabilities of the laboratory model control board and the features of hardware modeling on model boards. The 74 series of microcircuits is used.

The material of the methodological guidelines posted on the Internet resource for SRC is used. Practical part during work in the lessonroom

1. Familiarize yourself with the purpose of the pins and input/output signals of the control board.
2. Study the purpose of the main pins and signals of the microcircuits used in the control board.
3. Build a logical system for forming a sequence of a 4-bit binary code at the counter output with indication of the counter output signals using LED indicators and a 7-segment indicator with a common anode.
4. According to the task option, build a binary-decimal code converter to a 7-segment indicator code with a common cathode for 2 segments and implement the circuit on a model.

Prepare a protocol and save it in the corresponding task folder on the Moodle platform.

Practical part for independent work

Tasks and control questions for self-assessment are available on the Internet information resource for SRC: http://iot.kpi.ua/lms/

Laboratory work 2. Creating a project in Quartus CAD using graphical circuit input

Theoretical part

Studying the Quartus CAD interface using the example of designing a digital device (CPU) on a programmable logic integrated circuit (PLIC) using the graphical circuit input method.

The material of the methodological guidelines posted on the Internet resource for SRC is used. Practical part during work in the lesson room

Write down the logic function according to the given option and create a project in Quartus CAD using graphical circuit input. Check the result using simulation, draw conclusions, and answer the control questions.

Complete the protocol and save it in the appropriate task folder on the Moodle platform.

Assignments for independent work

Assignments and control questions for self-assessment are available on the Internet information resource for SRC: http://iot.kpi.ua/lms/

Laboratory work 3. Minimization of logical functions using Karnaugh maps and their implementation on 74 series microcircuits

Theoretical part

Acquire skills in minimizing logical functions using Karnaugh maps and practical implementation of minimized functions on 74 series microchips.

Use the material from Lecture 3 and Internet resources for independent study.

Practical part during work in the lesson room

Consider a function of 4 variables defined on sets of arguments (according to the variant).

1. Minimize the logical function using Karnaugh maps and construct logical circuits in I-NOT and OR-NOT bases.
2. Assemble the circuit on a breadboard (in one of the bases: AND-NOT or OR-NOT) using mounting boards, jumpers, and 74 series microcircuits.
3. Write down the logical function of 4 variables according to the given option and create a project in Quartus CAD, using the description of the circuit in Verilog HDL for the device being designed.
4. Check the result using simulation, paying attention to delays in the actual micro circuit, and draw conclusions.
5. Prepare a report on the results.

Complete the report and save it in the appropriate task folder on the Moodle platform.

Assignments for independent work

Tasks and control questions for self-assessment are available on the Internet information resource for SRC: http://iot.kpi.ua/lms/

Laboratory work 4. Designing a CPU on a multiplexer with a description in Verilog

Theoretical part

Acquiring skills in designing a CPU on a multiplexer with a description of its behavior and the structure of the multiplexer in Verilog HDL.

Lecture 6 material and Internet resources for independent study are used.

Practical part during work in the lesson room

1. Build a logic device circuit on KR1533KP2 microchips.
2. Provide a logical description of the circuit in Verilog using the case structure. Complete the protocol and save it in the appropriate task folder on the Moodle platform.

Assignments for independent work

Tasks and control questions for self-assessment are available on the Internet resource for SRC: http://iot.kpi.ua/lms/

Laboratory work 5. Modeling digital circuits using parametric elements

Theoretical part

Gaining experience in using parametric elements in QUARTUS II CAD, experimental research of counters built on their basis. Parametric elements (LPM function) are the use of ready-made mega functions of the design system to implement various CPUs. These functions have a finite number of parameters that are set by the user, depending on the required technical characteristics of the device being designed.

The material from Lecture 11 from the Internet resource for SRC is used.

Practical part during work in the lesson room

1. Design an electrical circuit for a synchronous counter with an arbitrary counting module for the parametric

elements of the QUARTUS II CAD system, which is specified in the table of task options.

2. Check the operation of the circuit in the signal editor, answer the control questions. Complete the protocol and save it in the appropriate task folder on the Moodle platform. Tasks for independent work Tasks and control questions for self-assessment are available on the Internet resource for SRC: http://iot.kpi.ua/lms/

Laboratory work 6. Behavioral description in Verilog when designing counters

Theoretical part

The material from Lecture 11 and the Internet resource for SRC is used. Practical part during work in the lesson room

1. Perform synthesis of a synchronous counter on a JK flip-flop with a counting module according to the task option.
2. Create a project in QUARTUS II CAD.
3. Use simulation to check the operation of the implemented counter.
4. Perform synthesis of an asynchronous counter on a JK flip-flop with a counting module according to the task option.
5. Create a project in QUARTUS II CAD.
6. Use simulation to check the operation of the implemented asynchronous counter. Prepare a report and save it in the appropriate task folder on the Moodle platform. Tasks for independent work

Tasks and control questions for self-assessment are available on the Internet information resource for SRC: http://iot.kpi.ua/lms/

Laboratory work 7. Designing synchronous digital Mil and Moore automata

Theoretical part

In this work, you need to construct a directed graph of a synchronous CA (Mil or Moore), which allows you to identify a specific sequence of binary symbols.

Use the material from Lecture 13 and the Internet resource for independent study. Practical part during work in the lesson room

Construct a directed graph of a digital automaton to identify a code combination of binary symbols specified by the corresponding option.

1. Describe the resulting graph in Verilog.
2. Perform a simulation of the implemented CA.

Prepare a report and save it in the appropriate task folder on the Moodle platform.

Assignments for independent work

Tasks and control questions for self-assessment are available on the Internet information resource for SRC: http://iot.kpi.ua/lms/

Note: The duration of laboratory work is 4 hours. When performing laboratory work in a distance mode, the time for their completion may be adjusted upwards. In this case, the number of laboratory works may be reduced.

6. Independent work for higher education students

Independent work by students includes preparation for lesson room sessions by mastering lecture materials, studying basic and additional literature, and completing laboratory work.

Topics 1.

Preparation for modular control work (tests in distance learning).

Topic 2. Automation of logical function minimization.

Study plan for Laboratory Work 1–3.

Topic 3. Synthesis of logic circuits on multiplexers.

Study materials for Laboratory Work 4.

Topic 4. Sequential digital devices.

SRS for Laboratory Work 5.

Topic 6. Synthesis of synchronous and asynchronous digital automata.

SRS for Laboratory Work 6.

Topic 7. Mili and Moore digital automata.

SRS for Laboratory Work 7.

Completion of homework assignment (HCW). Preparation for the test.

POLICY AND CONTROL

7. Policy of the academic discipline (educational component)

7.1. Forms of work

Lectures are conducted using visual aids and methodological materials that are accessible to higher education students. Students receive all materials through the Moodle learning platform, e-mail, and campus. A Telegram group is used for communication and consultations.

Higher education students are involved in discussing the lecture material and ask questions about its essence.

When performing laboratory work, individual and collective work forms (teamwork, pair work) are used to implement the teacher's tasks for acquiring independent practical work skills.

During the course, active and collective learning strategies are used, which are determined by the following methods and technologies:

1. problem-based learning methods (problem-based presentation, partial search (heuristic discussion), and research methods);
2. personality-oriented (developmental) technologies based on active forms and methods of teaching ("brainstorming," "situation analysis," etc.), discussion method;
3. information and communication technologies that ensure the problem-solving and research-oriented nature of the learning process and the activation of independent work by higher education students (electronic presentations, the use of computer- and multimedia-based practical tasks (tests), supplementing traditional lessons with interactive tools based on network communication capabilities (software, mobile applications, etc.);
4. explanatory and illustrative methods.

7.2. Rules for attending lessons

lessons can be held in lesson rooms according to the schedule lessons can also be held remotely in asynchronous mode using the Moodle learning platform with unique identification of the higher education student. Online lessons must be provided for by a corresponding order of Igor Sikorsky KPI.

If there are valid reasons, the student must notify the teacher in advance (1 day in advance) of the reasons for the possible absence from the test. All tests in distance learning mode are conducted synchronously (simultaneously for all students).

If it was not possible to notify in advance, the higher education applicant must contact the teacher within one week to agree on the form and procedure for eliminating the debt.

If a lesson room session falls on a non-working day (holiday, commemorative day, etc.), the material of such a session is partially transferred to the category "Independent work of higher education students" and partially added to the next session.

7.3. Rules for awarding incentive and penalty points

Bonus points:

+10 points – to the student author of an article (conference report) on the subject of the course (only if a set of materials is submitted).

The total number of incentive points cannot exceed 10 points. Penalty points:

-1 point for delay in submitting the LP protocol (more than 2 weeks) and absence from laboratory work without valid reasons.

8. University policy

8.1. Academic Integrity Policy

The policy and principles of academic integrity are defined in Section 3 of the Code of Honor of the National Technical University of Ukraine "Igor Sikorsky Kyiv Polytechnic Institute." For more details, see: https://kpi.ua/code

8.2. Standards of ethical conduct

The standards of ethical conduct for students and employees are defined in Section 2 of the Code of Honor of the National Technical University of Ukraine "Igor Sikorsky Kyiv Polytechnic Institute." Details https://kpi.ua/code

ASSESSMENT AND CONTROL MEASURES

9. Types of control and the learning outcomes assessment rating system (RS)

9.1. Types of control

Type of control	*Method of control*
Ongoing control	1. Modular control work (testing). 2. Completion and defense of homework assignments. 3. Completion and defense of laboratory work.
Calendar control	Conducted twice per semester to monitor the current status of syllabus requirements
Semester control	Credit

9.2. Rating system for assessing learning outcomes

Assessment is carried out according to the rating system set out in the syllabus.

The main part of the student's rating is formed through active participation in laboratory work, obtaining the results of modular control work (tests) and completing homework assignments. Modular control work and credit are conducted by a lecturer - a teacher of the Department of Radio Engineering Systems**.**

1) Ongoing assessment

Quick quizzes on the topic of the lesson, test assignments, discussion of legal cases, preparation of draft documents

The student's rating consists of points received for quick polls on the topic of the lesson, discussion of legal cases, solving practical tasks, supplementing the answers of other students in the process of discussion during practical lessons, completing online test assignments, and preparing draft documents. If a student is absent from a lab session, they must make up the missed lesson. Completion of all lab work is a prerequisite for receiving a positive grade for the course.

1. Laboratory work

Weighting score – 5.

Assessment criteria:

- complete task completion – 5;
- completion of the task, but insufficient theoretical knowledge – 4
- task completed, but no report – 1-3;
- work not completed – 0.

The maximum number of points for all laboratory work is 5x7 = 35 points.

2. Module test (MT)

Weighting score – 25.

Assessment criteria for offline learning:

- complete answers to all questions and complete task completion (at least 90%) – 22-25 points;
- sufficiently complete answer and complete task completion (at least 75%), or complete with minor errors – 19–21 points;
- incomplete answer (at least 60%) and minor errors – 14–18 points
- unsatisfactory performance of the task (does not meet the requirements) – 0 points.

Note: In distance learning, modular control is replaced by tests: 15 tests (maximum score for each – 1-2).

3. Homework control work (HCW) **Weighting – 10 points.** Assessment criteria:

- complete performance of the task (at least 90%) – 9-10 points;
- sufficiently complete completion of the task (at least 75%), or complete with minor errors – 6–8 points;
- incomplete completion of the task (at least 60%) – 4-5 points;
- incomplete task completion (less than 60%) – 1-3 points;
- task not completed – 0 points.

The maximum number of points for the HCW is 13 points.

If academic dishonesty is detected (collective completion of the HCW – "team contract"), the points received for the HCW are divided equally among the members of the "team."

Note:

Penalty and incentive points for (the sum of both penalty and incentive points shall not exceed $0.1r_C$ (4 points):

- absence from a laboratory lesson without valid reasons 1
- participation in the modernization, support, and administration of the discipline, completion of tasks to improve methodological and didactic materials for the discipline +1…+2

Overall rating score for the discipline (maximum 100 points):

$$R_{\Sigma} = R_{\text{ЛР}} + R_{\text{МКР}} + R_{\text{ДКР}},$$

$R_{\text{ЛР}}$ – rating points for completing laboratory work №1…№9 (from 0 to 35 points);

$R_{\text{МКР}}$ – rating points for modular control works (for distance learning – tests) (from 0 to 25 points);

$R_{\text{ДКР}}$ – rating points for home control work (from 0 to 10 points).

The rating scale for the discipline (without the test) is:

$$R = 35_{\text{LR}} + 25_{\text{MODULE TEST}} + 10_{\text{HCR}} = 70 \text{ points}$$

If, at the beginning of the last day of the semester, the number of points earned is not less than 60, the student can already receive a grade or increase their points by $R_{\text{ЗКР}}$ – a rating point for a test (ЗКР) in a discipline (from 0 to 30 points).

2) Calendar control

Carried out twice per semester as monitoring of the current status of syllabus requirements

Criterion	*First*	*Second*
Term	*Week 8*	*14th week*
Conditions for obtaining a positive result	if the current rating score is at least 50% of the maximum possible score at the time of the calendar contact role	if the current rating score is at least 50% of the maximum possible score at the time of the calendar control calendar control

3) Credit test

The maximum rating score without taking into account the final test is 100 points.

If a higher education applicant does not satisfy the required number of points, the results of the rating assessment are not canceled, but are normalized to 70 points, and the higher education applicant writes a final qualification work in the discipline, the points for which are added to the normalized points.

In distance learning, the final qualification work is performed in the form of a test.

In offline learning, the final qualification work is assessed out of 30 points in accordance with the assessment system:

– "excellent", complete answer (at least 90% of the required information) – 25–30 points;

– "good", sufficiently complete answer (at least 75% of the required information, or minor inaccuracies) – 20 24 points;

– "satisfactory", incomplete answer (at least 60% of the required information and some errors) – 15. 19 points;

– "unsatisfactory," unsatisfactory answer – 0 points.

Note: In distance learning, the final exam is conducted in the form of a test (30-60 questions).

The test is conducted on the Moodle distance learning platform, and questions can be of various types that can be implemented in Moodle.

4) Table of correspondence between rating points and university scale grades

Number of points	**Grade**
95	Excellent
85	Very good
75	Good
65	Satisfactory
60	Sufficient
Less than 60	Unsatisfactory

10. Additional information on the discipline (educational component)

Examples of tasks for laboratory work and independent research projects

A 5-variable function is defined on sets of arguments. Minimize the logical function using Karnaugh maps and construct logical circuits in I-NOT and OR-NOT bases. Describe the resulting functions in Verilog for implementation on PLIS.

Table of options.

No.	Function true	False function	Function undefined
1	1,2,4,9,11,2,27,31	0,3,10,15,17,18,19,20	
2		9,10,11,12,14,15,20,21,22	1, 3, 4, 6, 7, 25, 26, 27
3	1,2,3,7,8,9,19,20,21,22	0,13,14,15,16,17,19,30	
4		1,8,10,11,17,18,24,25,26,29	0,2,14,15,20,21
5	5,7,11,13,15,21,27,28,30	6,8,9,10,14	
6	7,9,10,12,14,17,19,21,22,29	1, 2, 4, 6, 8, 18, 26, 27, 31	
7	2, 4, 5, 6, 8, 14, 26, 27, 28, 30		1,7,11,12,21,22
8	0,4,5,6,7,8,9,17,20,21		1, 2, 3, 24, 25, 27, 28, 29
9	2, 3, 8, 19, 21, 27, 29		4,5,6,7,9,11,12,17
10	2, 3, 5, 8, 9, 15, 16, 17		1,4,10,11,13,14,21,22
11	7,8,9,10,11,12,17,18,19,20		1, 2, 3, 4, 5, 16, 29, 30, 31
12	2, 3, 8, 11, 14, 15, 23, 25, 28, 29	17, 18, 19, 20, 30, 31	
13	3, 14, 19, 23, 27, 31		11, 12, 15, 17, 18, 20, 21
14		8, 12, 13, 14, 15, 19, 21, 23	1, 2, 3, 10, 27, 29, 30
15	1, 7, 9, 11, 13, 15, 18, 19, 20	2, 3, 4, 10, 12, 14, 21, 27	
16		2,4,6,7,11,24,25,27,30	0,3,10,12,15,17,20,21
17	5,8,19,21,27,29,30	2, 3, 12, 14, 18, 24	
18	0,1,2,3,7,8,9,10,14,17,21		4,5,11,12,23,24,25
19	1,2,7,8,9,29,30		3,4,10,11,19,24,28,31
20		3, 14, 19, 23, 27, 28, 31	11, 12, 18, 20, 22, 25
2		0, 2, 3, 8, 19, 21, 27, 28, 29	4,5,6,11,12,16,17,18
2	3,5,6,9,13,14,18,24,28,29		1,7,8,19,21,22,31
2		1, 3, 4, 12, 14, 19, 23, 28, 31	5,7,8,10,21,22,25
24	8, 11, 14, 16, 23, 24, 25, 29, 30		4,6,17,18,19,20,21
25	3, 14, 15, 16, 19, 23, 27, 31		11, 12, 17, 20, 21
2		2, 8, 11, 14, 16, 23, 25, 29, 31	4, 6, 17, 18, 19, 20
27	1, 2, 4, 9, 13, 15, 17, 18, 19	3,5,7,12,24,25,26,31	
2	0,2,10,11,12,14,15,23,28	17, 19, 20, 21, 22, 24, 25, 26	
29	4,7,9,11,23,27,29		10, 14, 15, 16, 17, 19
30	2, 4, 8, 10, 11, 12, 13, 14, 17		16, 19, 20, 21, 23, 24, 25, 26

Task 2-1

Build a logic device on KR1533KP2 microcircuits, at the output of which a high signal level appears if the input 6-bit binary number is divisible by 3 or 4. Describe the resulting device in Verilog.

Task 2-2

Build a logic device on KR1533KP2 microchips, the output of which is a high signal level if the input 6-bit binary number is divisible by 4 or 5. Describe the resulting device in Verilog.

Task 2-3

Build a logic device on KR1533KP2 microcircuits, at the output of which a high signal level appears if the input 6-bit binary number is divisible by 5 or 6 or 7. Describe the resulting device in Verilog.

Task 2-4

Build a logic device on KR1533KP2 microcircuits, at the output of which a high signal level appears if the input 6-bit binary number is divisible by 3 or 5. Describe the resulting device in Verilog.

Tasks 2-5

Build a logic device on KR1533KP2 microchips, the output of which is a high signal level if the input 6-bit binary number is divisible by 5, 7, or 8. Describe the resulting device in Verilog.

Task 2-6

Build a logic device on KR1533KP2 microcircuits, at the output of which a high signal level appears if the input 6-bit binary number is divisible by 4 or 7. Describe the resulting device in Verilog.

Task 2-7

Build a binary-to-decimal code converter with a bit weight of 5-4-2-1 into a seven-segment indicator code on KR1533KP2 microcircuits (consider functions A and B). Describe the resulting device in Verilog.

Task 2-8

Build a binary-decimal code converter with a weight of 5-4-2-1 on KR1533KP2 microcircuits into a seven-segment indicator code (consider functions C and D). Describe the resulting device in Verilog.

Task 2-9

Build a binary-to-decimal code converter with a bit weight of 5-4-2-1 into a seven-segment indicator code on KR1533KP2 microcircuits (consider functions E and F). Describe the resulting device in Verilog.

Task 2-10

Build a binary-decimal code converter with a weight of 8-4-2-1 into a seven-segment indicator code on KR1533KP2 microcircuits (consider functions A and B). Describe the resulting device in Verilog.

Task 2-11

Build a binary-to-decimal code converter with a weight of 8-4-2-1 into a seven-segment indicator code on KR1533KP2 microcircuits (consider functions C and D). Describe the resulting device in Verilog.

Task 2-12

Build a binary-to-decimal code converter with a weight of 8-4-2-1 into a seven-segment indicator code on KR1533KP2 microcircuits (consider functions E and F). Describe the resulting device in Verilog.

Task 2-13

Build a converter from binary code to five-digit John-Son code on KR1533KP2 microchips. Describe the resulting device in Verilog.

Task 2-14

Build a converter from a five-digit Johnson code to binary code on KR1533KP2 microchips. Describe the resulting device in Verilog.

Task 2-15

Build devices on KR1533KP2 microcircuits that implement majority functions of 5 and 6 arguments. (A majority function is equal to "1" if half or more of the arguments are equal to "1"). Describe the resulting device in Verilog.

Task 2-16

Build devices on KR1533KP2 microchips that implement inverse majority functions of 5 and 6 arguments. (An inverse majority function is equal to "1" if half or more of the arguments are equal to "0"). Describe the resulting device in Verilog.

Task 2-17

Build a Gray code to binary code converter on KR1533KP2 microchips:

0 – 0000	4 – 0110	8 – 1100	12 – 1010
1 – 0001	5 – 0111	9 – 1101	13 - 1011
2 – 0011	6 – 0101	10	14 - 1001
3 – 0010	7 – 0100	11	15 – 1000

Describe the resulting device in Verilog.

Task 2-18

Build a Gray code to binary-decimal code converter on KR1533KP2 microcircuits:

0 – 0000	4 – 0110	8 – 1100	12 – 1010
1 – 0001	5 – 0111	9 - 1101	13 - 1011
2 – 0011	6 – 0101	10	14 - 1001
3 – 0010	7 – 0100	11	15 – 1000

Describe the resulting device in Verilog.

Task 2-19

Build a binary code to Gray code converter on KR1533KP2 microcircuits:

0 – 0000	4 – 0110	8 – 1100	12 – 1010
1 – 0001	5 – 0111	9 – 1101	13 - 1011
2 – 0011	6 – 0101	10	14 - 1001
3 – 0010	7 – 0100	11	15 – 1000

Describe the resulting device in Verilog.

Task 2-20

Build a binary-decimal code to Gray code converter on KR1533KP2 microcircuits:

0 – 0000	4 – 0110	8 – 1100	12 – 1010
1 – 0001	5 – 0111	9 – 1101	13 - 1011
2 – 0011	6 – 0101	10	14 - 1001
3 – 0010	7 – 0100	11	15 – 1000

Describe the resulting device in Verilog.

Task 2-21

Build a converter of a 4-bit straight binary code to a complementary code on KR1533KP2 microcircuits, provided that the most significant bit is sign.

Describe the resulting device in Verilog.

Task 2-22

Build a 4-bit complement binary code to straight code converter on KR1533KP2 microcircuits, provided that the most significant bit is significant. Describe the resulting device in Verilog.

Task 2-23

Build a 4-bit direct binary code converter from a negative number to a complement code on KR1533KP2 microcircuits, provided that there is no sign bit. Describe the resulting device in Verilog.

Task 2-24

Build a 4-bit two's complement code converter on KR1533KP2 microcircuits.

negative number into a straight code, provided that there is no sign bit. Describe the resulting device in Verilog.

Verilog.

Task 2-25

Build a converter of code 2 from 5 into binary code on KR1533KP2 microcircuits:

0 – 11000
1 – 00011
2 – 00101
3 – 00110
4 – 01001
5 – 01010
6 – 01100
7 – 10001
8 – 10010
9 – 10100

Describe the resulting device in Verilog.

Task 2-26

Build a converter from binary code to code 2 out of 5 on KR1533KP2 microchips:

0 – 11000
1 – 00011
2 – 00101
3 – 00110
4 – 01001
5 – 01010
6 – 01100
7 – 10001
8 – 10010
9 – 10100

Describe the resulting device in Verilog.

Task 2-27

Build a binary-decimal code converter with a weight of 2-4-2-1 on KR1533KP2 microcircuits into a seven-segment indicator code (consider functions A and B).

Describe the resulting device in Verilog.

Task 2-28

Build a binary-decimal code converter with a weight of 2-4-2-1 on KR1533KP2 microcircuits into a seven-segment indicator code (consider functions C and D).

Describe the resulting device in Verilog.

Task 2-29

Build a binary-to-decimal code converter with a weight of 2-4-2-1 on KR1533KP2 microcircuits into a seven-segment indicator code (consider functions E and F).

Describe the resulting device in Verilog.

Task

Build a converter on KR1533KP2 microcircuits that converts binary code with an excess of 3, which is formed by adding 0011_2 to each binary digit code, into a seven-segment indicator code. Describe the resulting device in Verilog.

Task 3

Synthesize a subtracting (summing) synchronous counter circuit with a counting module M=9 on JK flip-flops KR1533TV6 (TV9, TV10), using the specified states from 0 to 8. Construct timing diagrams for the circuit operation, check the counter for stability, and, if necessary, modify the circuit to ensure its stability. Perform circuit synthesis, starting with the initial setting of the trigger states when the power supply is turned on.

Describe the resulting device in Verilog.

Task options

No.	Counter type	M	Trigger type	States
1	Subtractive	14	KR1533TV6	0
2	Additive	13	KR1533TV9	1-13
3	Subtractive	12	KR1533TV10	2-13
4	Additive	11	KR1533TV6	2-12
5	Subtractive	10	KR1533TV9	3-12
6	Additive	9	KR1533TV10	3-11
7	Subtractive	14	KR1533TV6	1-14
8	Additive	13	KR1533TV9	0-12
9	Subtractive	12	KR1533TV10	1-12
10	Additive	11	KR1533TV6	3-13
11	Subtractive	10	KR1533TV9	4-13
12	Additive	9	KR1533TV10	6-14
13	Subtractive	14	KR1533TV6	2-15
14	Additive	13	KR1533TV9	2-14
15	Subtractive	12	KR1533TV10	3-14
16	Additive	11	KR1533TV6	5-15
17	Subtractive	10	KR1533TV9	5-14
18	Additive	9	KR1533TV10	7-15
19	Subtractive	14	KR1533TV6	0-13
20	Additive	13	KR1533TV9	2-14
21	Subtractive	12	KR1533TV10	4-15
22	Additive	11	KR1533TV6	4-14

23	Subtractive	10	KR1533TV9	6-15
24	Additive	9	KR1533TV10	2-10
25	Subtractive	14	KR1533TV6	1-14
26	Additive	13	KR1533TV9	0-12
27	Subtractive	12	KR1533TV10	0-11
28	Additive	11	KR1533TV6	0-10
29	Subtractive	10	KR1533TV9	0
30	Additive	9	KR1533TV10	1-9

Task 4

Synthesize a circuit for a subtracting (summing) **asynchronous** counter with a given counting module on JK triggers of the KR1533 series, using the given states. Synthesize the circuit, starting with the initial setting of the trigger states when the power supply is turned on. Describe the resulting counter circuit in Veri-log language.

Task 5-1

Using a minimum number of RS flip-flops, construct a Moore automaton circuit that allows you to detect the word **SOS** in the received sequence of letters. The letters (**S** = 001, **O** = 110) are transmitted in serial code, starting with the most significant bit. Describe the digital automaton circuit in Verilog.

Task 5-2

Using the minimum number of RS flip-flops, construct a Moore state machine circuit that allows you to detect the word **COD** in the received sequence of letters. The letters (C = 001, O = 101, **D** = 110) are transmitted in serial code, starting with the most significant bit. Describe the digital state machine circuit in Verilog.

Task 5-3

Using a minimum number of RS flip-flops, construct a Moore state machine circuit that detects the word **END** in the received sequence of letters. The letters (E=001, N=011, D=110) are transmitted in serial code, starting with the most significant digit. Describe the digital state machine circuit in Verilog.

Task 5-4

Using the minimum number of RS flip-flops, construct a Moore state machine circuit that allows you to detect the word **OFF** in the received sequence of letters. The letters (**F** = 011, **O** = 001) are transmitted in serial code, starting with the most significant bit. Describe the digital state machine circuit in Verilog.

Task 5-5

Using the minimum number of RS flip-flops, construct a Moore state machine circuit that allows you to detect the word **ERR** in the received sequence of letters. The letters (**E** = 001, **R** = 110) are transmitted in serial code, starting with the most significant bit. Describe the digital state machine circuit in Verilog.

Task 5-6

Using the minimum number of RS flip-flops, construct a Mealy machine circuit that allows you to detect the word **DOC** in the received sequence of letters. The letters (D = 010, O = 001, C = 101) are transmitted in serial code, starting with the most significant bit. Describe the digital machine circuit in Verilog.

Task 5-7

Using a minimum number of RS flip-flops, construct a Milie automaton circuit that allows you to detect the word **ISK** in the received sequence of letters. The letters (S=110, I=010, K=100) are transmitted in sequential code, starting with the most significant digit. Describe the digital automaton circuit in Verilog.

Tasks 5-8

Using the minimum number of RS flip-flops, construct a Mily automaton circuit that allows you to find the word **RED** in the received sequence of letters. The letters (R=010, E=000, D=110) are transmitted in serial code, starting with the most significant bit. Describe the digital automaton circuit in Verilog.

Task 5-9

Using the minimum number of RS flip-flops, construct a Milner automaton circuit that allows you to find the word **OUT** in the received sequence of letters. The letters (U=101, O=010, T=111) are transmitted in serial code, starting with the most significant bit. Describe the digital automaton circuit in Verilog.

Task 5-10

Using a minimum number of RS flip-flops, construct a Milie automaton circuit that allows you to find the word **KNC** in the received sequence of letters. The letters (K=010, N=111, C=011) are transmitted in sequential code, starting with the most significant digit. Describe the digital automaton circuit in Verilog.

Tasks 5-11

Using the minimum number of RS flip-flops, construct a Moore automaton circuit that allows you to find the word **ARG** in the received sequence of letters. The letters (A=011, R=101, G=001) are transmitted in serial code, starting with the most significant bit. Describe the digital automaton circuit in Verilog.

Task 5-12

Using the minimum number of RS flip-flops, construct a Moore state machine circuit that allows you to find the word **SIN** in the received sequence of letters. The letters (S=011, I=010, N=110) are transmitted in serial code, starting with the most significant bit. Describe the digital state machine circuit in Verilog.

Task 5-13

Using the minimum number of RS flip-flops, construct a Moore automaton circuit that allows you to find the word **COS** in the received sequence of letters. The letters (C=011, O=111, S=001) are transmitted in serial code, starting with the most significant digit from the senior category. Describe the digital machine diagram in Verilog language.

Tasks 5-14

Using a minimum number of RS flip-flops, construct a Moore automaton circuit that can detect the word **ARC** in a received sequence of letters. The letters (A=011, R=001, C=101) are transmitted in serial code, starting with the most significant bit. Describe the digital automaton circuit in Verilog.

Task 5-15

Using the minimum number of RS flip-flops, construct a Moore state machine circuit that allows you to find the word **BIN** in the received sequence of letters. The letters (B=011, I=101, N=010) are transmitted in serial code, starting with the most significant bit. Describe the digital state machine circuit in Verilog.

Task 5-16

Using a minimum number of RS flip-flops, construct a Milie automaton circuit that allows you to find the word **PIK** in the received sequence of letters. The letters (P=100, I=101, K=010) are transmitted in sequential code, starting with the most significant digit. Describe the digital automaton circuit in Verilog.

Task 5-17

Using the minimum number of RS flip-flops, construct a Mily automaton circuit that allows you to find the word **KCI** in the received sequence of letters. The letters (K=100, C=011, I=101) are transmitted in serial code, starting with the most significant digit. Describe the digital automaton circuit in Verilog.

Task 5-18

Using the minimum number of RS flip-flops, construct a Mily automaton circuit that allows you to find the word **RID** in the received sequence of letters. The letters (R=100, I=010, D=110) are transmitted in serial code, starting with the most significant bit. Describe the digital automaton circuit in Verilog.***Task 5-19***

Using a minimum number of RS flip-flops, construct a Milie automaton circuit that allows you to detect the word **MMX** in the received sequence of letters. The letters (M=100, X=110) are transmitted in sequential code, starting with the most significant digit. Describe the digital automaton circuit in Verilog.

Task 5-20

Using a minimum number of RS flip-flops, construct a Milner automaton circuit that allows you to find the word **PEN** in the received sequence of letters. The letters (P=100, E=110, N=111) are transmitted in serial code, starting with the most significant digit. Describe the digital automaton circuit in Verilog.

Task 5-21

Using the minimum number of RS flip-flops, construct a Moore automaton circuit that allows you to find the word **INT** in the received sequence of letters. The letters (I=101, N=011, T=010) are transmitted in serial code, starting with the most significant bit. Describe the digital automaton circuit in Verilog.

Task 5-22

Using the minimum number of RS flip-flops, construct a Moore automaton circuit that allows you to find the word **CTO** in the received sequence of letters. The letters (C=101, T=010, O=111) are transmitted in serial code, starting with the most significant bit.
from the senior category. Describe the digital machine diagram in Verilog language.

Task 5-23

Using a minimum number of RS flip-flops, construct a Moore automaton circuit that can detect the word **DEC** in a received sequence of letters. The letters (D=101, E=001, C=110) are transmitted in serial code, starting with the most significant digit. Describe the digital automaton circuit in Verilog.

Task 5-24

Using the minimum number of RS flip-flops, construct a Moore automaton circuit that allows you to detect the word **MIC** in the received sequence of letters. The letters (M=101, I=011, C=001) are transmitted in serial code, starting with the most significant bit. Describe the digital automaton circuit in Verilog.

Task 5-25

Using a minimum number of RS flip-flops, construct a Moore state machine circuit that can detect the word **CHIP** in a received sequence of letters. The letters (C=101, I=100, P=011) are transmitted in serial code, starting with the most significant digit. Describe the digital state machine circuit in Verilog.

Task 5-26

Using the minimum number of RS flip-flops, construct a Mealy machine circuit that allows you to find the word **ORG** in the received sequence of letters. The letters (O=110, R=101, G=111) are transmitted in serial code, starting with the most significant bit. Describe the digital machine circuit in Verilog.

Task 5-27

Using the minimum number of RS flip-flops, construct a Mily automaton circuit that allows you to find the word **3IP** in the received sequence of letters. The letters (3=110, I=100, P=010) are transmitted in serial code, starting with the most significant bit. Describe the digital automaton circuit in Verilog.

Task 5-28

Using a minimum number of RS flip-flops, construct a Milly automaton circuit that allows you to find the word **DNA** in the received sequence of letters. The letters (D=110, H=011, K=100) are transmitted in sequential code, starting with the most significant digit. Describe the digital automaton circuit in Verilog.

Task 5-29

Using the minimum number of RS flip-flops, construct a Mily automaton circuit that allows you to find the word **BIG** in the received sequence of letters. The letters (B=110, I=010, G=111) are transmitted in serial code, starting with the most significant bit. Describe the digital automaton circuit in Verilog.

Task 5-30

Using the minimum number of RS flip-flops, construct a Mily automaton circuit that allows you to find the word **CON** in the received sequence of letters. The letters (C=110, O=001, N=101) are transmitted in serial code, starting with the most significant bit. Describe the digital automaton circuit in Verilog.

Working program of the academic discipline (syllabus):

Compiled:

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Approved by:

Meeting of the Department of Radio Engineering Systems (Minutes No. 6/25 dated June 26, 2025)

Approved by:

Methodological Commission of the Radio Engineering Faculty (Minutes No. 06/2025 dated 26.06.2025)